Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 1. This sheet, which includes Fig. 1, replaces the original sheet including Fig. 1. Figure 1 is now labeled as "Prior Art."

Attachment: Replacement Sheet

REMARKS

Claims 1-4, 6-8, 11-13, 15-21 and 23 are pending. Claims 1, 7 and 16 are amended herein. The Applicant respectfully requests reconsideration of the Claims in light of the amendments and the discussion set forth below.

35 U.S.C. §103

Claims 1-4, 6-8, 11-13, 15-21 and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kadanka et al. (U.S. Patent No. 5,621,308) in view of Mietus (U.S. Patent No. 5,666,046). Applicants have reviewed the recited references and respectfully submit that the present invention, as is recited in Claims 1-4, 6-8, 11-13, 15-21 and 23, is neither anticipated nor rendered obvious by Kadanka and Mietus, either alone or in combination.

The Examiner's attention is respectfully directed to independent Claim 1 which recites that an embodiment of the Applicant's invention includes a band-gap reference circuit, comprising:

> ...a band-gap reference unit; buffer circuit electronically coupled with said band-gap reference unit; and a single component voltage pull-up device electronically coupled between said band-gap reference unit and said buffer circuit, wherein said single component voltage pull-up device acts to reduce a required supply voltage to maintain a band-gap reference voltage and wherein said single component voltage pull-up device is implemented as a transistor with a V_{BE} of less than 1.0 volts.

Claims 7 and 16 contain limitations similar to those contained in Claim 1. Claims 2-4, and 6 depend from claim 1 and recite further features of the claimed invention. Claims 8, 11-13 and 15 depend from claim 7 and recite further features of the claimed invention. Claims 15-21 and 23 depend from claim 7 and recite further features of the claimed invention.

Kadanka in view of Mietus does not teach or suggest all of the limitations of Claim 1. Specifically, the primary reference Kadanka does not teach important limitations of the Claims and the secondary reference Mietus does not teach or suggest a modification of Kadanka that would remedy it's deficiencies. Applicant respectfully submits that Kadanka et al. does not anticipate or render obvious a band-gap reference circuit that includes "a single component voltage pull-up device electronically coupled between said band-gap reference unit and said buffer circuit, wherein said single component voltage pull-up device acts to reduce a required supply voltage to maintain a band-gap reference voltage and wherein said single component voltage pull-up device is implemented as a transistor with a V_{BE} of less than 1.0 volts" as is recited in Claim 1 (Claims 7 and 16 contain similar limitations).

Kadanka et al. only shows an electrical apparatus for providing a reference signal that includes a regulator portion that provides a substantially constant current. It is important to note that Kadanka et al. simply does not discuss a buffer circuit or a voltage pull-up device such as is set forth in Claim 1 (Claims 7 and 16 contain similar limitations). The Applicant respectfully submits that the Examiner has equated components of the Kadanka et al. system with the buffer circuit and the voltage pull-up device that have disclosed functions that are substantially different from those recited in Claim 1 as attributable to the buffer circuit and the voltage pull-up device.

For example, Kadanka et al. discloses that element 54, cited in the Office Action as being equivalent to the recited buffer circuit, is actually a part of "band-gap reference 72." Moreover, Kadanka et al discloses that element 70, cited in the Office Action as being equivalent to the recited voltage pull-up device, is actually the "regulator portion" of voltage reference circuit 39.

It is important to note that in order to meet all the limitations of the Claims, the components that are equated to elements of the Claims must have the functionality of the claim elements to which they are equated. There is no teaching or suggestion that element 54 "acts to reduce a required supply voltage" as is required to meet the limitations of Claim 1. If the Examiner intends to maintain the current rejection, the Applicant respectfully requests that the Examiner point out where in the cited references this limitation is taught or suggested.

Applicant respectfully submits that nowhere in the Kadanka et al. reference is a single component voltage pull-up device that is electronically coupled between a band-gap reference unit and a buffer circuit, that acts to reduce a required supply voltage to maintain a band-gap reference voltage, and is implemented as a transistor with a V_{BE} of less than 1.0 volts as is set forth in Claim 1 and disclosed in the Applicant's specification, taught or suggested. Consequently, the embodiments of the Applicant's invention as are set forth in Claims 1, 7 and 16 are neither anticipated nor rendered obvious by Kadanka et al.

As alluded to above, Mietus does not teach or suggest a modification of Kadanka et al. that would remedy the deficiencies of Kadanka et al. outlined above. More specifically, Mietus does not teach or suggest a band-gap reference circuit that includes "a single component voltage pull-up device electronically coupled between and located intermediate to said band-gap reference unit and said buffer circuit, wherein said single component voltage pull-up device acts to reduce a required supply voltage to maintain a band-gap reference voltage and wherein said single component voltage pull-up device is implemented as a transistor with a V_{BE} of less than 1.0 volts" as is recited in the Claims. Applicant respectfully submits that nowhere in the Mietus reference is a single component voltage pull-up device that is electronically coupled between a

band-gap reference unit and a buffer circuit, that acts to reduce a required supply voltage to maintain a band-gap reference voltage, and is implemented as a transistor with a V_{BE} of less than 1.0 volts as is set forth in Claim 1 and disclosed in the Applicant's specification taught or suggested. Consequently, the embodiments of the Applicant's invention as are set forth in Claims 1, 7 and 16 are neither anticipated nor rendered obvious by Kadanka et al. in view of Mietus.

Therefore, Applicant respectfully submit that Kadanka et al. in view of Mietus does not anticipate or render obvious the present claimed invention as recited in Claims 1, 7, and 16 and, as such, the 35 U.S.C. § 103 rejection of Claims 1, 7, and 16 is improper. Accordingly, Applicant respectfully submits that Claims 1, 7, and 16 are in condition for allowance. In addition, Applicant respectfully submits that Kadanka et al. in view of Mietus does not anticipate or render obvious the present invention as is recited in Claims 2-4 and 6 which depend from independent Claim 1, Claims 8, 11-13 and 15 which depend from independent Claim 7, and Claims 15-21 and 23 which depend from independent Claim 16, and that Claims 2-4, 6, 8, 11-13, 15-21 and 23 are also in condition for allowance as being dependent on an allowable base claim.

CONCLUSION

In light of the foregoing amendments and remarks, Applicant respectfully submits that the remaining claims are in condition for allowance. Applicant respectfully requests allowance of the pending Claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

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Respectfully submitted,

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